VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain [coupled to a] configured to receive said first supply voltage, and (iii) a first source coupled to [an] a first output; and

a first resistive element having (i) a first side coupled [between] to said first source and (ii) a second side configured to receive said second supply voltage, wherein said apparatus [provides voltage tolerance between said input voltage and said output] is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage.

2. (AMENDED) The apparatus according to claim 1, wherein said [apparatus is further configured to provide fail-safe protection between said input voltage and said output] input voltage ranges up to twice said first supply voltage with respect to said second supply voltage.

3. (AMENDED) The apparatus according to claim 1, wherein said first device is configured in a source-follow configuration.

4. (AMENDED) The apparatus according to claim 1, wherein said first device comprises an NMOS device.

5. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a native NMOS device.

7. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a PMOS device.

8. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a native PMOS device.

11. (AMENDED) A method for implementing voltage protection comprising the steps of:

configuring a device to have (i) a gate for receiving an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a drain for receiving [a] said first supply voltage, and (iii) a source [for presenting] coupled to an output; and

configuring a resistive element [between] to have (i) a first side coupled to said source and (ii) a second side for receiving said second supply voltage, wherein said device [provides voltage tolerance between said input voltage and said output] and said resistive element are arranged such that a maximum voltage

drop across a gate oxide of said device does not exceed a difference between said first supply voltage and said second supply voltage.

12. (AMENDED) The method according to claim 11, wherein said [method is further configured to provide fail-safe protection between said input voltage and said output] input voltage ranges up to twice said first supply voltage with respect to said second supply voltage.

18. (AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain [coupled] configured to [a] receive said second [first] supply voltage, and (iii) a first source coupled to a first output, and (B) a first resistive element having (i) a first side coupled [between] to said first source and (ii) a second side configured to receive said first [second] supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate coupled to said first output, (ii) a second drain [coupled] configured to receive said first supply voltage, and (iii) a second source coupled to a second output, and (B) a second

resistive element having (i) a first side coupled [between] to said second source and (ii) a second side configured to receive said [first] second supply voltage, wherein said apparatus [provides voltage tolerance between said input voltage and said output] is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage.

19. The apparatus according to claim 1, further comprising:

a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain configured to receive said second supply voltage, and (iii) a second source coupled to a second output;

a second resistive element having (i) a first side coupled to said second source and (ii) a second side configured to receive said first supply voltage; and

a multiplexer configured to multiplex [wherein] said first output and said second output [are multiplexed] to [present] a third output.

20. (AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging

from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain [coupled] configured to [a] receive said first supply voltage, and (iii) a first source coupled to an output, and (B) a first resistive element having (i) a first side coupled [between] to said first source and (ii) a second side configured to receive said second supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain [coupled] configured to receive [a] said second [first] supply voltage, and (iii) a second source coupled to said output, and (B) a second resistive element having a first side coupled [between] to said second source and a second side configured to receive said first [second] supply voltage, wherein said apparatus [provides voltage tolerance between said input voltage on said output] is arranged such that a maximum voltage drop across each gate oxide of said first device and said second device does not exceed a difference between said first supply voltage and said second supply voltage.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus generally comprising a first device and a first resistive element. The first device generally comprises (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain configured to receive the first supply voltage, and (iii) a first source coupled to a first output. The first resistive element may have (i) a first side coupled to the first source and (ii) a second side configured to receive the second supply voltage. The apparatus is generally arranged such that a maximum voltage drop across a gate oxide of the first device does not exceed a difference between the first supply voltage and the second supply voltage.

SUPPORT FOR CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example on page 5 lines 4-7, page 5 line 19 through page 6 line 16, page 7 line 15 through page 8 line 2, page 8 lines 8-11, page 10 line 20 through page 11 line 18, and FIGS. 5, 6, 10, 12 and 13 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1, 11, 18 and 20 under 35 U.S.C. §112, second paragraph, has been obviated, in part, by appropriate amendment and traversed, in part, and should be withdrawn.

Regarding claims 5, 8 and 16-17, a native device is defined in the specification. In particular, page 8, line 16 through page 9, line 8 defines a native device as a device with a threshold at or near 0 volts. Also see, for example, U.S. Patent No. 4,831,589 for additional details of native devices, which are known to one skilled in the art.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(e) as being anticipated by Taguchi '855 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Okamura '536 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Akira JP41120504 has been obviated by appropriate amendment and should be withdrawn.

Okamura discloses an intermediate potential generating circuit having output stabilizing circuit (Title). Taguchi discloses reference voltage generator circuit using source

followers (Title). Akira discloses a semiconductor circuit (Title). Okamura, Taguchi and Akira each do not appear to disclose or suggest every element arranged as presently claimed. As such, the pending claims are fully patentable over the cited references and the rejections should be withdrawn.

In particular, claims 1, 11, 18 and 20 provide a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage. Okamura, Taguchi and Akira each appear to disclose an input voltage at the transistor gates ranging between a power supply voltage and ground (or Vss). Therefore, Okamura, Taguchi and Akira each do not appear to teach or suggest a first device comprising (i) a first gate configured to receive an input voltage ranging from **greater than a first supply voltage** to at least a second supply voltage as presently claimed. As such, the pending claims are fully patentable over the cited references and the rejections should be withdrawn.

Pending claim 18 provides (A) a first stage comprising (ii) a first drain configured to receive a second supply voltage and (iii) a first source coupled to a first output and (B) a second stage comprising (i) a second gate coupled to the first output and (ii) a second drain configured to receive a first supply voltage. Okamura, Taguchi and Akira each appear to be silent regarding a second stage having a the **drain of a first device** coupled to a

second voltage source and the **drain of a second device** coupled to a first voltage source. Therefore, Okamura, Taguchi and Akira each do not appear to teach or suggest (A) a first stage comprising (ii) a first drain configured to receive a second supply voltage and (iii) a first source coupled to a first output and (B) a second stage comprising (i) a second gate coupled to the first output and (ii) a second drain configured to receive a first supply voltage as presently claimed. As such, the pending claim is fully patentable over the cited reference and the rejections should be withdrawn.

Pending claim 20 provides (A) a first device comprising (i) a first gate configured to receive an input voltage and (iii) a first source coupled to an output, (B) a first resistive element having (i) a first side coupled to the first source, (C) a second device comprising (i) a second gate configured to receive the input voltage and (iii) a second source coupled to the output, and (D) a second resistive element having a first side coupled to the second source. Okamura, Taguchi and Akira each appear to be silent regarding two devices and two resistive elements arranged as in the claim 20. FIGS. 26 and 27 of Okamura disclose two transistors having common gate nodes and common drain nodes but lack the resistive elements. Therefore, Okamura, Taguchi and Akira each do not appear to teach or suggest (A) a first device comprising (i) a first gate configured to receive an input voltage and (iii) a first source coupled to an output, (B) a first resistive element having

(i) a first side coupled to the first source, (C) a second device comprising (i) a second gate configured to receive the input voltage and (iii) a second source coupled to the output, and (D) a second resistive element having a first side coupled to the second source as presently claimed. As such, the pending claim is fully patentable over the cited reference and the rejections should be withdrawn.

Regarding pending claims 5, 8 and 16-17, the references appear silent regarding native devices. In particular, Applicant's representative has downloaded an electronic version of Taguchi and Okamura from the United States Patent and Trademark Office (USPTO) database (www.uspto.gov). A search for the word "native" had no occurrences. Therefore, the references are also silent regarding native devices. While, Akira does not appear to be available electronically in English, Akira also appears to be silent regarding native devices. As such, none of the references appear to disclose or suggest a native device as presently claimed and the rejection should be withdrawn.

Furthermore, the Examiner is respectfully requested to refrain from omnibus rejections that simply list all of the pending claims and then asserts that the claims are disclosed somewhere among one or more figures in the references (see MPEP 707.07(d)). As such, Applicants' representative respectfully requests that any subsequent rejections regarding the pending claims be presented in

a non-final Office Action, since no reasonable opportunity has been provided for a first respond to the rejection(s).

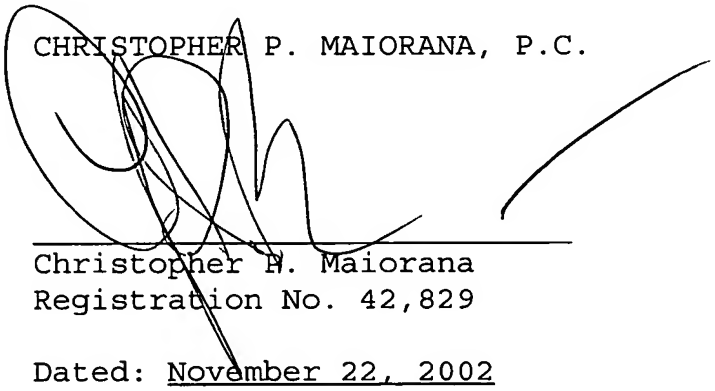
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829

Dated: November 22, 2002

c/o Peter Scott
Intellectual Property Law Department
LSI Logic Corporation
1551 McCarthy Boulevard, M/S D-106
Milpitas, CA 95035
Docket No.: 02-0003 / 1496.00201